III-Vs from a logical point of view

Low-cost mass-consumer electronics products are based on the performance boost enabled by shrinking transistor sizes. To continue progress in this direction, changes in the structure and composition of these devices will be needed in the next few years. One proposal, III-V channels, has been the basis of much recent work. Dr Mike Cooke reports on research presentations on this theme at December's IEEE International Electron Devices Meeting (IEDM 2008).

As silicon becomes more difficult to shrink, new channel materials are being considered. In the near term, strained silicon or silicon germanium — possibly in new structures (e.g. fully depleted, silicon-on-insulator, FinFET) — are likely to be used, but longer term a whole gear shift is probably needed. Devices made with III-V compound semiconductors such as InGaAs and InSb deposited on silicon have already been successfully demonstrated.

These efforts are designed to enable continued use of the scaling formula of the complementary metal oxide semiconductor devices (CMOS) that dominate the mass electronics markets: mobile phones (apart from the transmit power amplifier), entertainment, video and still imaging, PCs and peripherals, etc. Improvements are sought in the directions of higher speed, higher functionality and lower power dissipation.

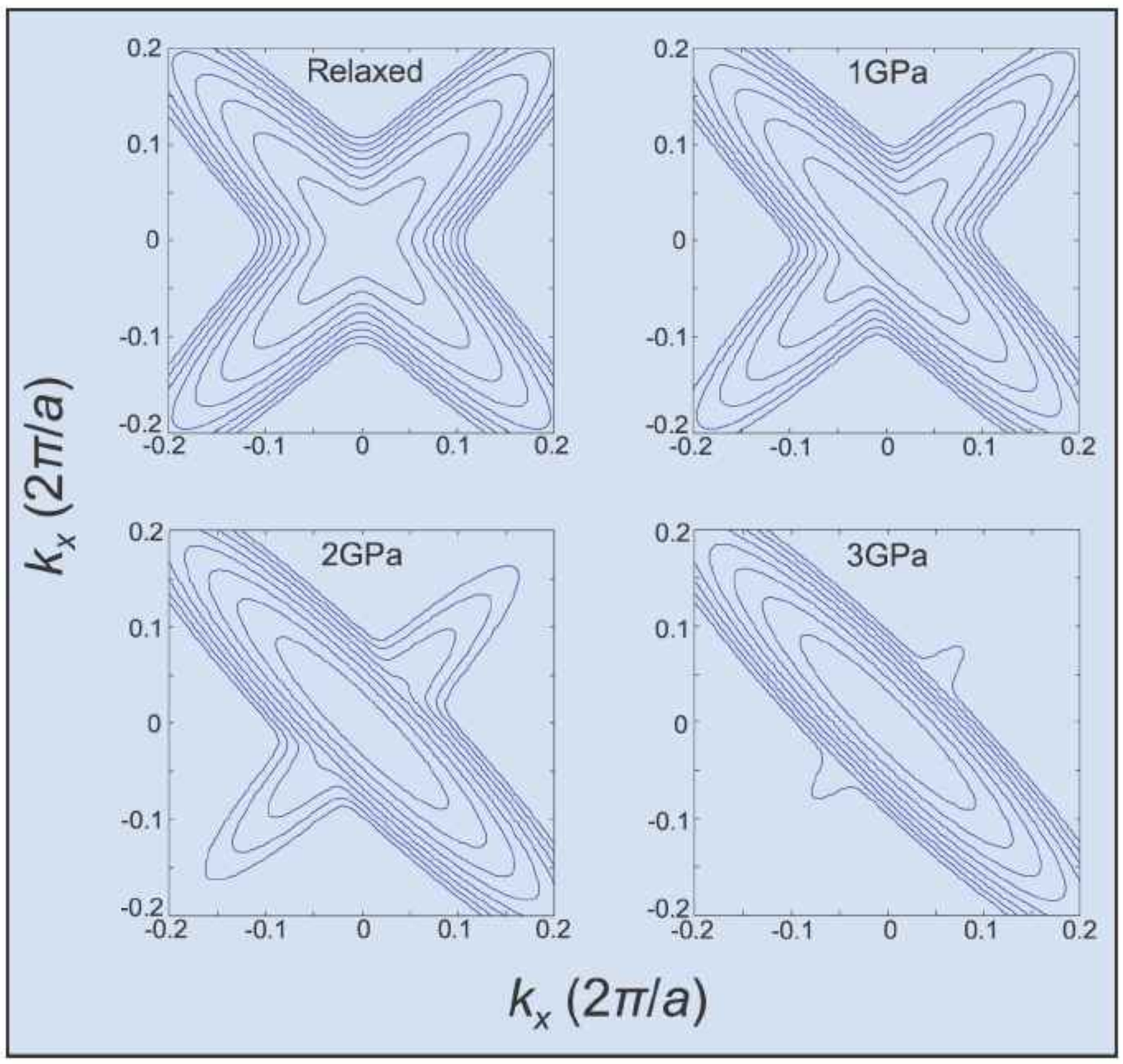

Figure 1. Energy-contours for holes in k-space for differing values of compressive stress in Si.

Carrier boosts

Antoniadis and Khakifirooz from MIT [1] surveyed the present use of uniaxial strained silicon, and of prospective alternatives, for maintaining the carrier velocity enhancement needed to scale down electronic technology. The two main alternatives are germanium and/or some compound semiconductor consisting of III-V material combinations.

The main effect of straining silicon is to modify the conduction and valence band structures (Figure 1). These modifications alter the way electrons and holes respond to electric fields. CMOS devices use both electron and hole transport to achieve their tasks in NMOS and PMOS transistors. Traditional local strain engineering methods can create strains up to about 0.5%. This can be increased to 1% with the use of preferential relaxation of biaxial strain. This creates a mobility enhancement of about 100%; a value that is maintained at low temperatures, suggesting that it is the velocity of the carriers that is increased (reduced effective mass) in the mobility formula. The other main factor in increased mobility — reduced scattering — is usually temperature dependent. Short-channel transistors based on the biaxial relaxation technique have yet to be built.

However, short-channel transistors built using uniaxial techniques can show mobility increases of up to 4x for holes and 8x for electrons, but the virtual source velocity of the carriers seems limited to a 2x improvement. For the hole velocity, this is explained by theoretical calculations showing that the critical region for determining the effective mass — the top of the valence band — does not change much once the stress reaches 2GPa (Figure 1). The increased mobility here is explained as being due to a reduction in inter-band scattering.

These factors are already impacting the improvements achieved at the 65nm and 45nm technology nodes. Intel, for example, is already producing devices for the market at 45nm, and the next stages are in the lab pipeline. To maintain development it is likely that drastic changes in the channel material will be needed.

The germanium option is mainly being developed with a view to its higher performance of hole transport. However, this will also need to be strained to achieve significant improvement over silicon. III-V channels are being developed for electron transport enhancement.

Unfortunately, the small effective mass needed for velocity enhancement usually comes with a narrow band gap, limiting the supply voltage that can be used. Antoniadis and Khakifirooz believe that special device design will be essential to realize the intrinsic electron transport benefits of III-V options. These designs will need to combine the reduced-drain electric field of the high-electron-mobility transistor (HEMT) architecture with the reduced resistance of source/drain self-alignment techniques.

A further problem to overcome will be the reduced inversion capacitance compared with silicon — this could limit potential drive currents and device performance. The researchers also point to previous work [2] showing that it will be parasitic rather than inversion capacitance that will be the main cause of switching delays in such devices. The conventional metric based on inversion capacitance is thus not relevant to the assessment of these structures.

Power dissipation is a further concern, particularly in highly dense devices. Antoniadis and Khakifirooz see reducing the supply voltage as being the main way to take advantage of enhanced carrier velocity materials and technologies. For some applications, but not all, the combination of low supply voltage (low power) and high performance is what is wanted. This is true for both battery-operated mobile and power-conserving devices.

Oxides for InGaAs

At the experimental level, the most recent stage in developing III-V MOSFETs has been to develop gate dielectric materials to reduce gate leakage while maintaining performance [3]. If the IEDM 2008 presentations

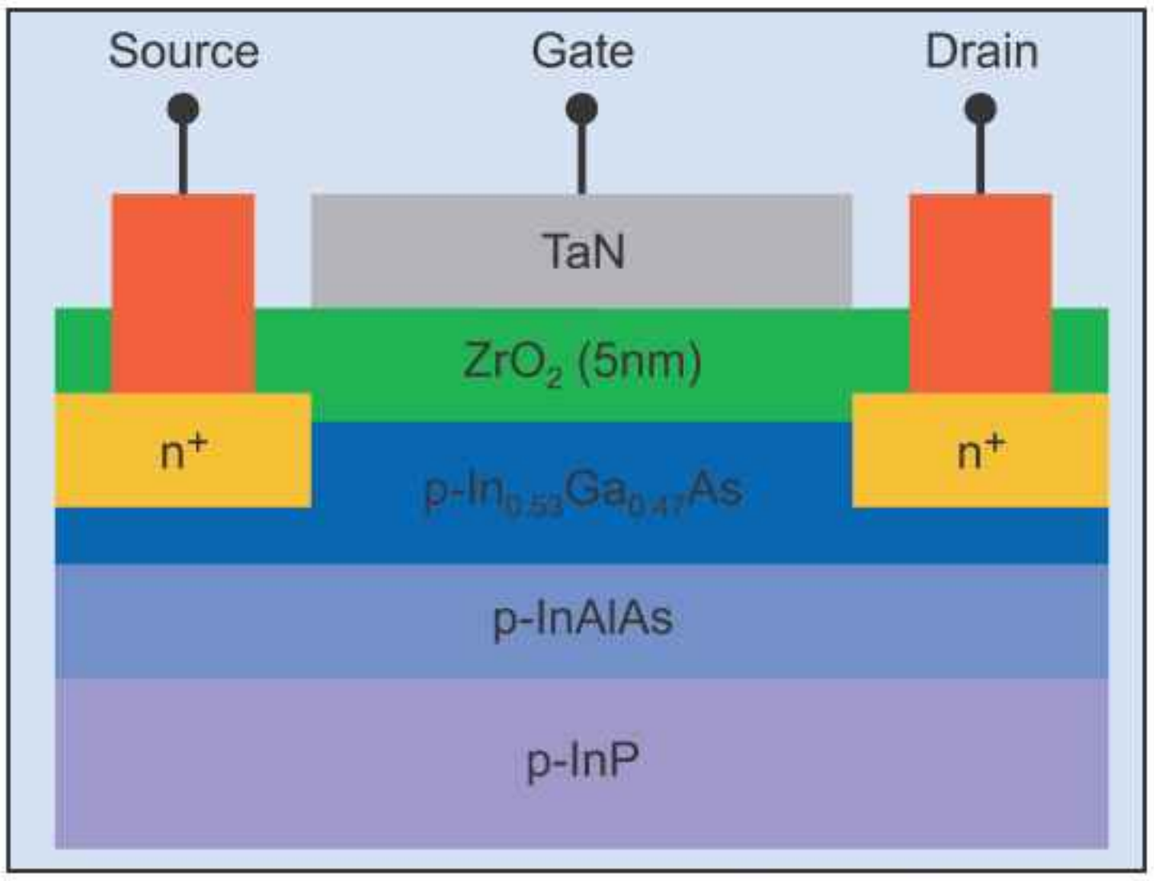

Figure 2. Schematic for an InGaAs device with ZrO_2 dielectric.

are any indication, most emphasis in the past year seems to have been placed on the indium gallium arsenide solution. Only one of the six papers in session 15 on 'III-V MOSFETs with High K Dielectrics' was not InGaAs based. Since the emphasis is on finding a decent oxide, the experimenters generally make life easier for themselves by using indium phosphide substrates, rather than adding the complicating factor of depositing InGaAs on silicon.

Collaborative work between Intel, SEMATECH, and the universities of Texas at Austin, New York at Albany, Stanford, and Oklahoma looked at 'Addressing the Gate Stack Challenge for High Mobility $In_xGa_{1-x}As$ Channels For NFETs' [4]. Various dielectrics were evaluated to determine equivalent oxide thickness (EOT) scalability for high performance and electrostatic control with acceptable leakage for a low off-current; the impact of charge trapping; thermal stability on InGaAs; and the impact of indium concentration on the interface quality for surface channel MOSFETs. Atomic layer deposition (ALD) techniques were used and the need for cleaning was shown to be minimal, in line with recent suggestions that ALD is self-cleaning.

MOS capacitor measurements on various gate stacks were carried out to assess the options: ZrO_2, HfO_2, Al_2O_3, and $Hf_xAl_{1-x}O$ (with x = 0.5 and 0.8). The ZrO_2 structure (Figure 2) was chosen for further study as having the most promise in scaling to a capacitive equivalent thickness (CET) of 0.5nm with low gate leakage current. It is also suggested that the ZrO_2 may undergo a phase change from its usual monoclinic structure to a tetragonal formation during the anneal process that increases its k value to 30. The gate stack also appears stable up to the temperatures required to activate the doping after implantation (~700°C).

Previous work with ZrO_2 suggests that the Fermi level is not strongly pinned at the dielectric-channel interface,

which is another prerequisite for effective MOSFETs. This is confirmed by the turn-on characteristics of transistors built in the new work (CET ~0.78nm). However, detailed characterization of interface states and charge trapping in the dielectric that can adversely impact performance has yet to be carried out and is considered 'imperative' to evaluating the potential of these stacks. It is found that a high indium concentration (>70%) reduces the transistor performance, suggesting degradation of the interface. It is believed that new passivation techniques will need to be developed to realize higher-mobility NMOSFETs from the material structure.

Purdue University has used ALD Al_2O_3 as a high-k gate dielectric in high-performance surface channel $In_{0.75}Ga_{0.25}As$ NMOSFETs [5]. The devices operate in inversion/enhancement mode — i.e. they are the normally-off type of MOSFET, as used in the mainstream CMOS industry.

Although the InGaN layers were grown using molecular beam epitaxy (MBE) on InP substrates, the high-k gate stack was deposited using ALD to bring the process closer to that seen in CMOS manufacturing. ALD processes favor Al_2O_3 or HfO_2 compared with more complicated combinations such as $Ga_2O_3(Gd_2O_3)$ that can be accessed with MBE deposition.

The devices demonstrated a maximum inversion current of 1.0A/mm and an electron velocity of $1.0x10^7$cm/s with a 0.75μm gate length and a source–drain voltage of 2V. The peak extrinsic transconductance was 430μS/μm. A systematic study of various indium concentrations ($In_{0.53}Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$ and $In_{0.75}Ga_{0.25}As$) suggests that indium-enriched InGaAs could be an ideal channel material for CMOS high-speed low-power logic application, the team says. The highest-indium-content device gives the best performance due to its narrow band gap of 0.52eV.

The I_{on}/I_{off} ratio is 10^6, which is a rather low value. The team attributes this to a large drain junction leakage current and believes this could be improved with more sophisticated junction engineering.

The Purdue team has also been studying the interface traps set up in the Al_2O_3 dielectric [6]. These are found to be at a relatively high level, but do not seem to affect the transistor performance unduly. It is suggested that the low impact of interface traps is due to their donor-like behavior, which does not pin the Fermi level.

Passivation

Singapore researchers have created a high-mobility enhancement-mode InGaAs NMOSFET using phosphine (PH_3) passivation and a TaN/HfO_2/InGaAs gate stack [7]. Experiments were also performed using devices with an HfAlO dielectric. Participants in the research included researchers from Singapore's National University (NUS) and the institutes of Microelectronics and of Materials Research and Engineering.

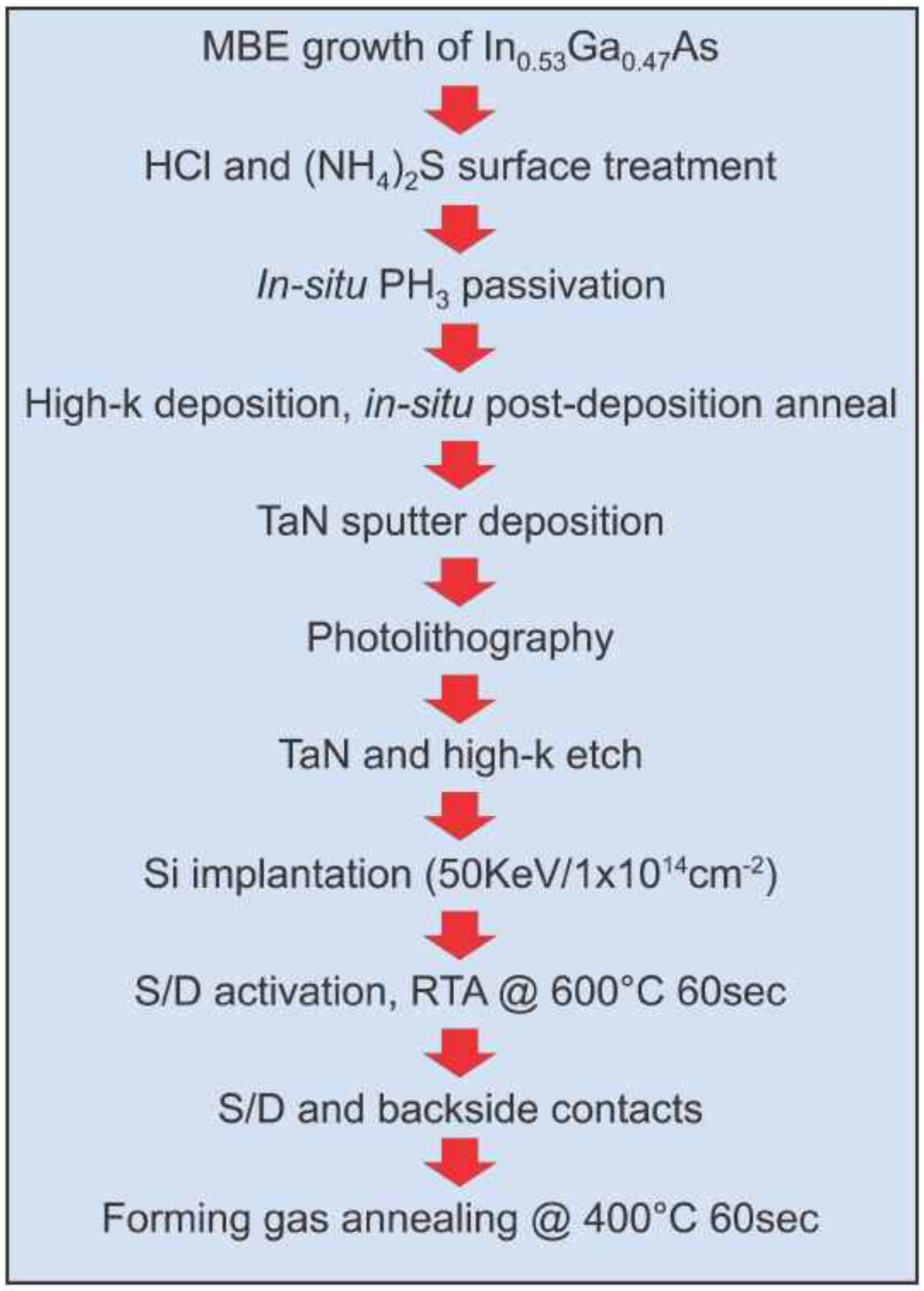

Figure 3. Process steps in Singapore's plasma PH_3-passivated high-mobility inversion InGaAs MOSFET with self-aligned gate-first process.

Of particular note is the use of a self-aligned process where the source–drain regions are formed by implantation after the gate stack is deposited, as used in traditional CMOS manufacturing (Figure 3). The success of such process flows depends on the stability of the gate stack during the high temperatures of the anneal process (600°C rather than >750°C, as used more normally) required to repair the implantation damage so that the silicon n-type doping chemicals can become activated. The p-type channel doping comes from Zn incorporated during initial InGaAs deposition.

Devices with and without PH_3 passivation were produced. One effect is to suppress the formation of arsenic oxide on the InGaAs surface, a factor believed to degrade the quality of the interface with the gate stack. High-frequency C–V measurements show that the interface trap density is reduced using PH_3 passivation (D_{it} = $8.6x10^{11}cm^{-2}eV^{-1}$ with passivation, and $4.3x10^{12}cm^{-2}eV^{-1}$ without).

Capacitance measurements on PH_3-passivated MOS structures give an effective oxide thickness (EOT) of 1.7–3.0nm and a gate leakage current of $2x10^{-5}/cm^2$ at a gate potential of 2V. The lower EOT was achieved

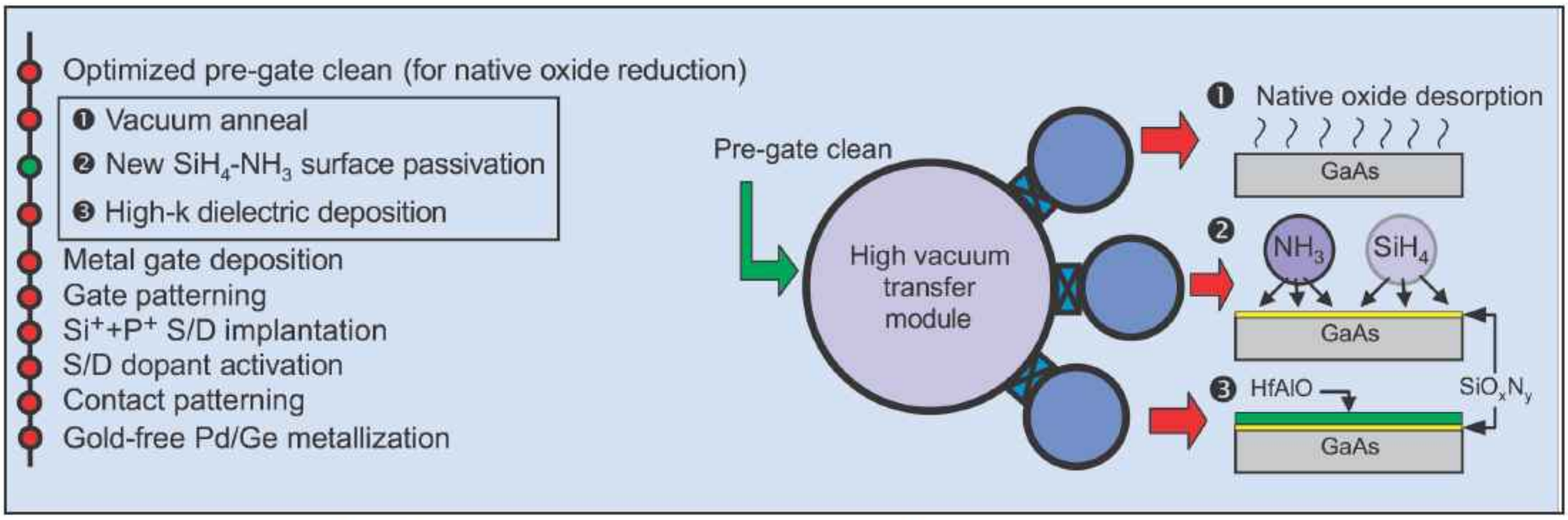

Figure 4. Process for fabricating inversion-type n-channel GaAs MOSFETs with SiH_4–NH_3 surface passivation.

by using a 5.5nm layer of HfAlO, while the higher figure came from a thicker 10nm layer of HfO_2. The gate stack maintains its stability through the rapid thermal anneal (RTA) step, showing a frequency spread of 1.3% in C–V measurements. The n^+ source/drain regions are created using silicon implantation. The effective mobility of the channel is 1600cm^2/Vs. A 95nm MOSFET was demonstrated with the gate-first technology, but without PH_3 passivation. This is claimed to be a first for the self-aligned gate-first technology that was used.

IBM's TJ Watson research center has been studying sub-100nm short-channel $In_{0.7}Ga_{0.3}As$ MOSFET scaling characteristics down to 80nm for both depletion- and enhancement-mode devices [8]. The researchers report good scaling of on-current, transconductance and virtual source velocity. A high current of 960μA/μm was achieved and a record transconductance of 793μS/μm is claimed.

National Tsing Hua University of Taiwan (together with two scientists from Intel and one from Purdue) has performed C–V measurements under light illumination and under a wide range of temperatures in order to study the interface quality of Al_2O_3/Ga_2O_3 stacks on n- and p- $In_{0.2}Ga_{0.8}As$/GaAs [9]. The interface is said to be of very high quality with a free-moving Fermi-level near the band-edges (the regions close to E_C and E_V).

Apart from InGaAs, another group from Singapore [10] reported on the use of a silane–ammonia gas mixture to passivate HfAlO high-k dielectric on GaAs (Figure 4). TaN was used as the metal gate. An interface state density D_{it} of ~1x $10^{11}eV^{-1}cm^{-2}$ is claimed, which is the lowest reported value for a high-k dielectric formed on GaAs by CVD, ALD, or PVD techniques. The technology was used to realize a 160nm gate-length enhancement-mode surface channel GaAs MOSFET. The peak electron mobility was measured at a high value of ~2100cm^2/Vs. The dielectric reliability was characterized by using bias-temperature instability (BTI) techniques.

Quantum wells

Intel and Qinetiq continue to promote InSb quantum well (QW) technology for logic applications [11]. This year, the QWFET structure was a 40nm compressively strained p-channel FET (Figure 5). The f_T cut-off was 140GHz with a 40nm gate length and 0.5V supply. This is claimed to be the highest f_T ever reported for III-V p-channel FETs. The transconductance (G_m) is 500μS/μm, which is also the highest reported value for such a device.

While III-Vs have impressive performance enhancements over Si MOSFETs for n-channel (both in terms of MOSFETs and for quantum well structures) the p-channel side tends to drag behind. As seen above, Ge is a promising candidate for filling the MOSFET gap, but for QWFETs parasitic conduction by different carriers (parallel conduction) is difficult to control in creating useful Ge-based devices. In III-Vs, p-channel QWFETs struggle to meet the performance of existing Si technology.

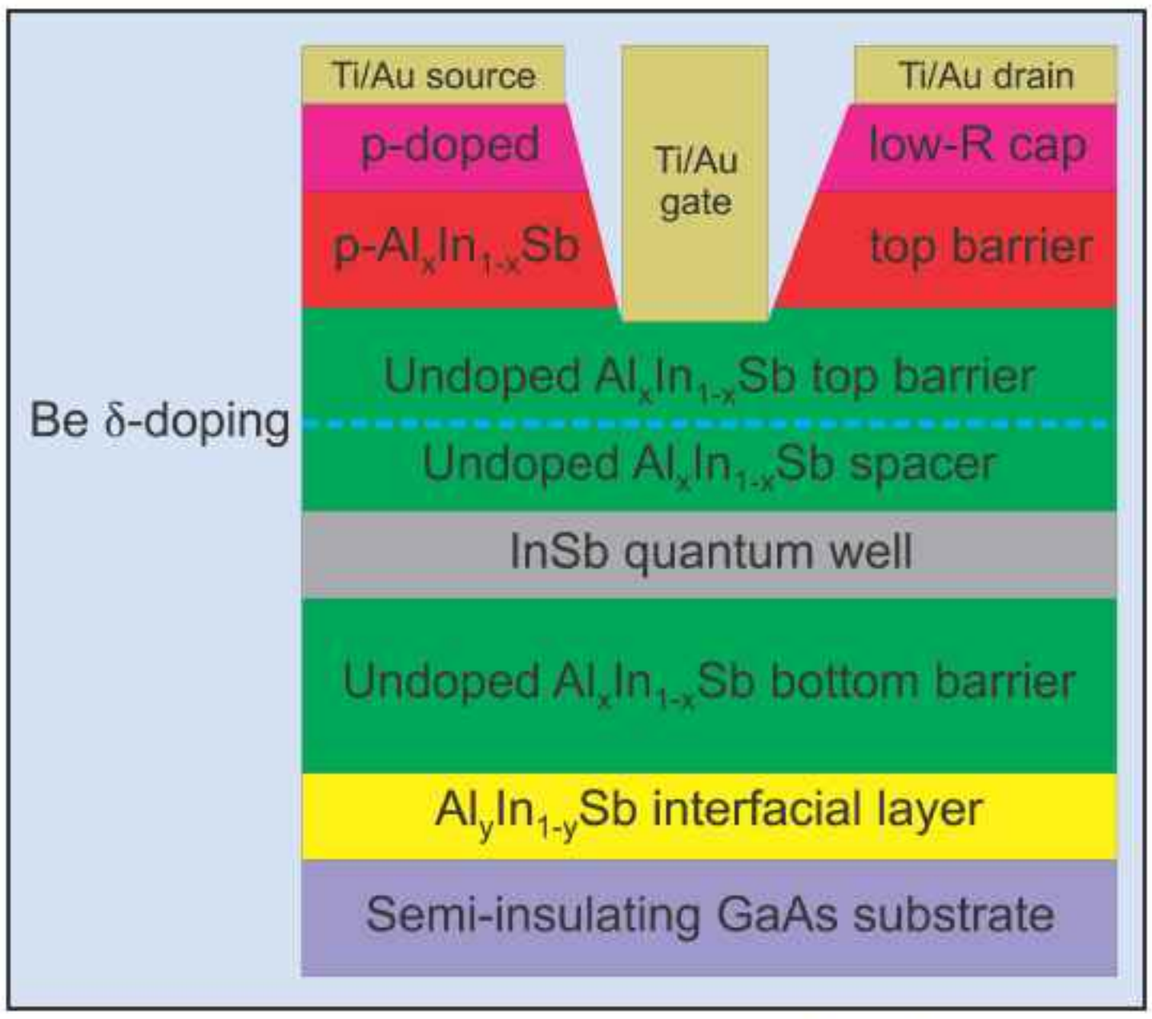

Figure 5. Intel/Qinetiq structure for p-QWFET built using InSb technology.

Intel and Qinetiq are attracted to indium antimonide (InSb) for this, given that this compound has the highest hole mobility of any III-V material. Theoretical investigations suggest that this compressive strain can significantly reduce the in-plane effective mass of the holes, thus increasing speeds and hence mobility in the material.

After some simulation work, the researchers have produced various structures with compressively strained InSb QWs. The strain is introduced by growing the InSb on $Al_xIn_{1-x}Sb$. By varying the Al concentration, different biaxial compressive strain values can be produced. Beryllium delta-doping above a spacer layer provides the carrier source for the QW channel (Figure 5). The advantage of using such remote doping is that there are then no ionized scattering centers to reduce the mobility in the channel. Using these techniques, the team has achieved a p-QW mobility of 1230cm^2/Vs at a carrier density of 1.1x10^{12}/cm^2 by using a biaxial compressive strain of 1.9% (InSb on $Al_{0.35}In_{0.65}Sb$). This is about 5x the mobility for suitably strained silicon. ■

References

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